REMARKS

The Examiner's Answer dated June 28, 2004, has been received and reviewed.

Claims 1-5, 11-17, 25-28, and 33-38 are currently pending and under consideration in the above-referenced application. In view of the remarks that have been presented in the Examiner's Answer, an RCE is being filed to withdraw the rejections of claims 1-5, 11-17, 25-28, and 33-38 above-referenced application from appeal and, thus, to reopen prosecution of the above-referenced application.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 102(e)

Claims 1-4, 11-14, 16, 25-27, 33-35, and 37 stand rejected under 35 U.S.C. § 102(e) for being drawn to subject matter which is allegedly anticipated by the subject matter described in U.S. Patent 5,712,185 to Tsai et al. (hereinafter "Tsai").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Tsai describes a method for forming shallow trench isolation structures in a semiconductor substrate. The method of Tsai includes providing a substrate 30 that includes a silicon oxide layer, which is referred to as "pad oxide layer 32," thereover, as well as a silicon nitride layer 34 over the pad oxide layer 32. FIG. 3A; col. 2, lines 53-58. A sacrificial layer 36 of either polysilicon or silicon oxide is formed over the silicon nitride layer 34. FIG. 3B; col. 2, line 59, to col. 3, line 2. A photomask 37 with apertures for defining trenches in the semiconductor substrate 30 is then formed over the sacrificial layer 36. FIG. 3C; col. 3, lines 3-4. Next, the trenches 38 are formed through each of layers 36, 34, and 32 and in the semiconductor substrate 30. FIG. 3D; col. 3, lines 19-23.

The photomask 37 is then removed and the silicon nitride layer 34A descumed, or etched laterally beneath the overlying sacrificial layer 36A. FIG. 3E; col. 3, lines 19-23. The sacrificial layer may then optionally be removed. Col. 3, lines 33 and 34.

Thereafter, a thin oxide layer 39 is formed on the surfaces of the semiconductor substrate 30 that are exposed within the trench 38A. FIG. 3F; col. 3, lines 34-38.

The trench 38A is filled with a suitable dielectric material, which is referred to as "isolation material 40," such as tetraethylorthosilicate (TEOS), which also fills the descumed regions of the silicon nitride layer 34B and forms a dielectric layer over the sacrificial layer 36A. FIG. 3G; col. 3, lines 38-50.

The dielectric layer and sacrificial layer 36A are then removed to expose the surface of the silicon nitride layer 34B and to form an isolation region 40A from the isolation material. FIG. 3H; col. 3, lines 51-56. Upon removal of the silicon nitride layer 34B, regions of the dielectric material that filled the descumed portion of the silicon nitride layer 34B extend laterally beyond the outer periphery of the trench 38A and over portions of the pad oxide layer 32A. FIG. 3I; col. 3, lines 57-60. Exposed portions of the pad oxide layer 32A are then removed from the surface of the semiconductor substrate 30, leaving only the isolation region 40A and portions of the pad oxide layer 32B that are shielded thereby. FIG. 3J; col. 3, lines 60-66.

Independent claim 1, as amended and presented herein, recites a method for forming an isolation structure that includes, among other things, etching a layered structure that includes a buffer film layer, an underlying dielectric layer, and a semiconductor substrate to form a trench. Once the trench has been formed, an oxide layer is formed on exposed portions of the semiconductor substrate. Thereafter, a portion of the buffer film layer is selectively etched.

In contrast to the subject matter to which amended independent claim 1 is drawn, Tsai lacks any express or inherent description of selectively etching the silicon nitride layer 34A thereof *following* the formation of the thin oxide layer 39 within the trench 38A. Rather, the description of Tsai is limited to descuming the silicon nitride layer 34A, optionally removing the sacrificial layer 36A, *then* forming the thick oxide layer 38 within the trench 38A. *See* FIGs. 3E and 3F.

In view of the limited disclosure of Tsai, it is respectfully submitted that Tsai does not anticipate each and every element of amended independent claim 1. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(e), amended independent claim 1 is drawn to subject matter which is allowable over the subject matter described in Tsai.

Claims 2-4 are each allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Independent claim 11, as amended and presented herein, also recites a method that includes selectively etching a buffer film layer *after* an oxide layer has been formed on exposed portion of a semiconductor substrate within a trench.

Again, Tsai lacks any express or inherent description of selectively etching the silicon nitride layer 34A thereof after the thin oxide film 39 has been formed within the trench 38A. Instead, Tsai describes descuming, or selectively etching, the silicon nitride layer 34A *before* the thin oxide film 39 is formed. *See* FIGs. 3E and 3F.

Therefore, Tsai does not anticipate each and every element of amended independent claim 11, as would be required to maintain the 35 U.S.C. § 102(e) rejection thereof.

Claims 12-14 and 16 are each allowable, among other reasons, for depending directly or indirectly from claim 11, which is allowable.

Independent claim 25, which has been amended to remove limitations and, thus, is now broader in scope, is directed to a method for forming an isolation structure on a semiconductor device structure that includes a semiconductor substrate with a trench formed therein and an oxide layer on portions of the semiconductor substrate within the trench. The method of independent claim 25 includes, among other things, selectively etching a portion of a buffer film layer located over the semiconductor substrate.

Tsai does not expressly or inherently describe selectively etching a portion of a buffer film layer that resides over a semiconductor substrate that includes a trench with an oxide layer therein. Rather, the description of Tsai is limited to descuming, or selectively etching, a silicon

nitride layer 38A of a semiconductor device structure that includes a trench *without an oxide layer therein*. *See* FIG. 3E.

Claims 26 and 27 are both allowable, among other reasons, for respectively depending directly and indirectly from claim 25, which is allowable.

Independent claim 33 has also been amended to remove limitations. Therefore, as amended, the scope of independent claim 33 has been broadened. The method of independent claim 33 includes selectively etching a portion of a buffer film layer of a semiconductor device structure to expose portions of an upper surface of an underlying dielectric layer that are adjacent to an upper edge of a trench of the semiconductor device structure. The act of selectively etching of independent claim 33 is effected on the buffer film layer of a semiconductor device structure that already includes an oxide layer on portions of the trench thereof.

In contrast, the descuming process (of silicon nitride layer 34B) described in Tsai does not occur until after the thin oxide film 39 is formed in the trench 38A. Therefore, Tsai does not expressly or inherently describe, or anticipate, each and every element of independent claim 33, as would be required in order to maintain the 35 U.S.C. § 102(e) rejection of independent claim 33.

Each of claims 34, 35, and 37 is allowable, among other reasons, for depending either directly or indirectly from claim 33, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1-4, 11-14, 16, 25-27, 33-35, and 37 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Claims 5, 15, 17, 28, 36, and 38 stand rejected under 35 U.S.C. § 103(a).

Tsai

Claims 17 and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai in view of the Examiner's Comment.

Claim 17 is allowable, among other reasons, for depending from claim 11, which is allowable.

Claim 38 is allowable, among other reasons, for depending from claim 33, which is allowable.

Tsai in View of Lee

Claims 5, 15, 28, and 36 each stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai in view of Lee HS, et al., "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)," 1996 IEEE Symposium on VLSI Technol. Dig. of Technical Papers, pages 158-59 (hereinafter "Lee").

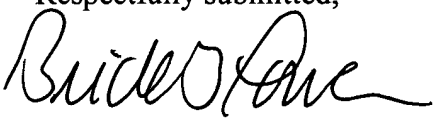
Claims 5, 15, 28, and 36 are each allowable, among other reasons, for depending from claims 1, 11, 25, and 33, respectively, each of which is allowable.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections of claims 5, 15, 17, 28, 36, and 38 is respectfully requested.

CONCLUSION

It is respectfully submitted that each of claims 1-5, 11-17, 25-28, and 33-38 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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Date: August 30, 2004
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